

5 What Is Claimed Is:

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1. An operational amplifier output stage, comprising:
✓ a pre-driver sub-stage and a final sub-stage,
the pre-driver sub-stage having a plurality of transistors being biased
10 by a plurality of current sources, the pre-driver sub-stage being adapted to accept a
current signal (δI_{in}) from an input g_m cell;
the pre-driver stage being further adapted to provide biasing to a plurality of
transistors in the final sub-stage; and
the pre-driver sub-stage being coupled to the final sub-stage so as to provide
15 current gain from input to output of $\delta I_o \approx \beta_n * \beta_p * \delta I_{in}$.

2. The operational amplifier output stage recited in Claim 1, further
comprising localized feedback circuitry enclosed in the output stage operable to
correct signal errors more rapidly than an overall amplifier feedback loop.

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✓ 3. The operational amplifier output stage recited in Claim 1, further
comprising localized feedback circuitry and inherent RHPZ cancellation operable to
extend bandwidth.

✓ 4. The operational amplifier output stage recited in Claim 1, wherein the
plurality of transistors in the final sub-stage comprises 4 transistors arranged as a
complementary pair of differential transistors.

5 ✓ 5. The operational amplifier output stage recited in Claim 1 for use in an integrated circuit.

✓ 6. The operational amplifier output stage recited in Claim 1 for use in a DSL driver.

✓ 7. The operational amplifier output stage recited in Claim 1, wherein the
10 pre-driver sub-stage comprises two circuits, the first pre-driver sub-stage circuit being adapted to condition a positive portion of an inputted signal for transfer to a first final sub-stage circuit of the final sub-stage, and the second pre-driver sub-stage circuit being adapted to condition a negative portion of an inputted signal for transfer to a second final sub-stage circuit of the final sub-stage;

15 the first pre-driver sub-stage circuit being coupled to the first final sub-stage circuit operable to amplify the positive portion of a signal in tandem; and

the second pre-driver sub-stage circuit being coupled to the second final sub-stage circuit operable to amplify the negative portion of a signal in tandem.

✓ 8. The operational amplifier output stage recited in Claim 7, wherein the
20 first final sub-stage circuit and the second final sub-stage circuit are interconnected at an output terminal node such that the conditioned and amplified positive portion of the signal and the conditioned and amplified negative portion of the signal are joined in phase with minimal crossover distortion the output signal (δI_o) having the form δI_o
 $\approx \beta_n * \beta_p * \delta I_{in}$.

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[illegible]

pre-driver sub-stage;

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to extend bandwidth.

~~Extend to~~

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connected to a sixth node for receiving a negative portion of an input signal,

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at the first node, and its base coupled at the second node;

coupled to a third node;

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5 a fourth transistor having its collector and base being coupled to a fourth node, and its emitter coupled to the first voltage supply rail V_{cc} at the first node;

a second voltage supply rail V_{ee} coupled to a fifth node;

a second pre-driver sub-stage circuit coupled to the sixth node, the second pre-driver sub-stage circuit further comprising:

10 a fifth transistor having its emitter coupled to the second voltage supply rail V_{ee} at the fifth node, and its base coupled to the sixth node;

a sixth transistor having its emitter coupled to the sixth node, its base coupled to a seventh node, and its collector coupled to the second node;

a seventh transistor having its base and collector coupled to a seventh node;

15 and its emitter coupled to an eighth node;

an eighth transistor having its collector and base being coupled to the eighth node, and its emitter coupled to the second voltage supply rail V_{ee} at the fifth node;

a cross connection between the second transistor's collector and the sixth transistor's emitter at the sixth node, and the second transistor's emitter and the sixth transistor's collector at the second node, the cross connection resulting in a

20 proportion of any error current flowing into the second transistor's emitter and sixth transistor's emitter to flow out through the second transistor's collector and the sixth transistor's collector into the base of the first transistor and the base of the fifth transistor;

5 a first current source coupled between the first voltage supply rail V_{cc} at the first node and the second node;

 a second current source coupled between the first voltage supply rail V_{cc} at the first node and the seventh node;

 a third current source coupled between the second voltage supply rail V_{ee} at
10 the fifth node and at the third node;

 a fourth current source coupled between the second voltage supply rail V_{ee} at the fifth node and the sixth node;

 a final sub-stage, comprising:

 a first final sub-stage circuit further conditioning the positive portion of the
15 current signal provided by the first pre-driver sub-stage circuit, the first final sub-stage circuit comprising:

 a ninth transistor having its emitter coupled to the first transistor's collector at a ninth node, and its base and collector coupled to a tenth node;

 a tenth transistor having its base coupled to the ninth node, and its collector
20 coupled to the first voltage supply V_{cc} rail at the first node;

 a second final sub-stage circuit further conditioning the negative portion of the current signal, provided by the second pre-driver sub-stage circuit, the second final sub-stage circuit comprising:

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5 an eleventh transistor having its emitter coupled to the fifth transistor's collector at an eleventh node, its base and collector coupled to the ninth transistor's base and collector at the tenth node;

a twelfth transistor having its base coupled to the eleventh node, and its collector coupled to the second voltage supply rail V_{cc} at the fifth node;

10 a twelfth node interconnecting the tenth transistor's emitter with the twelfth transistor's emitter; and

an output terminal coupled to the twelfth node.

11. The operational amplifier output stage recited in Claim 10 wherein the first, second, third, fourth, ninth and twelfth transistors are pnp transistors and the
15 fifth, sixth, seventh, eighth, tenth and eleventh transistors are npn transistors.

12. The operational amplifier output stage recited in Claim 10, including a localized feedback circuitry enclosed within the operational amplifier output stage.

13. The operational amplifier output stage recited in Claim 12, wherein the localized feedback circuitry utilizes current feedback principles operable to
20 substantially eliminate cross-over distortion.

14. The operational output stage recited in Claim 12, wherein the localized feedback system utilizes voltage feedback principles, operable to provide unity gain.

15. An operational amplifier output stage, comprising:
25 a first voltage supply rail V_{cc} connected to a first node;

5 two connection terminals to an input stage, a first terminal connected to a second node for receiving a positive portion of a current signal and a second terminal connected to a sixth node for receiving a negative portion of a current input signal;

a first pre-driver sub-stage circuit coupled at the second node, the first pre-driver sub-stage circuit further comprising:

10 a first transistor having its emitter coupled to the first voltage supply rail V_{cc} at the first node, and its base coupled at the second node;

a second transistor having its emitter coupled to the second node and its base coupled to a third node;

a third transistor having its base and collector coupled to the third node;

15 a fourth transistor having its collector and base being coupled to a fourth node, and its emitter coupled to the first voltage supply rail V_{cc} at the first node;

a second voltage supply rail V_{ee} coupled to a fifth node;

a second pre-driver sub-stage circuit coupled to the sixth node, the second pre-driver sub-stage circuit further comprising:

20 a fifth transistor having its emitter coupled to the second voltage supply rail V_{ee} at the fifth node, and its base coupled to the sixth node;

a sixth transistor having its emitter coupled to the sixth node, its base coupled to a seventh node, and its collector coupled to the second node;

a seventh transistor having its base and collector coupled to a seventh node;

25 and its emitter coupled to an eighth node;

5 an eighth transistor having its collector and base being coupled to the eighth node, and its emitter coupled to the second voltage supply rail V_{ee} at the fifth node;

a cross connection between the second transistor's collector and the sixth transistor's emitter at the sixth node, and the second transistor's emitter and the sixth transistor's collector at the second node, the cross connection resulting in a

10 proportion of any error current flowing into the second transistor's emitter and sixth transistor's emitter to flow out through the second transistor's collector and the sixth transistor's collector into the base of the first transistor and the base of the fifth transistor;

a first current source coupled between the first voltage supply rail V_{cc} at the

15 first node and the second node;

a second current source coupled between the first voltage supply rail V_{cc} at the first node and the seventh node;

a third current source coupled between the second voltage supply rail V_{ee} at the fifth node and at the third node;

20 a fourth current source coupled between the second voltage supply rail V_{ee} at the fifth node and the sixth node;

a final sub-stage, comprising:

a first final sub-stage circuit further conditioning the positive portion of the current signal provided by the first pre-driver sub-stage circuit, the first final sub-

25 stage circuit comprising:

5 a ninth transistor having its emitter coupled to the first transistor's collector at a ninth node, and its base coupled to a tenth node and its collector coupled to the second voltage supply rail V_{ee} at the fifth node;

a tenth transistor having its base coupled to the ninth node, and its collector coupled to the first voltage supply V_{cc} rail at the first node;

10 a second final sub-stage circuit further conditioning the negative portion of the current signal, provided by the second pre-driver sub-stage circuit, the second final sub-stage circuit comprising:

an eleventh transistor having its emitter coupled to the fifth transistor's collector at an eleventh node, its base coupled to the ninth transistor's base and
15 collector at the tenth node and its collector coupled to the first voltage supply rail V_{cc} at the first node;

a twelfth transistor having its base coupled to the eleventh node, and its collector coupled to the second voltage supply rail V_{ee} at the fifth node;

a twelfth node interconnecting the tenth transistor's emitter with the twelfth
20 transistor's emitter; and

an output terminal coupled to the twelfth node. \

16. The operational amplifier output stage recited in Claim 15, including a localized feedback circuitry enclosed within the operational amplifier output stage.

17. The operational amplifier output stage recited in Claim 16, wherein
25 the localized feedback circuitry utilizes current feedback principles.

5 18. The operational amplifier output stage in Claim 16, wherein the localized feedback circuitry utilizes voltage feedback principles.

 19. The operational amplifier output stage recited in Claim 15, wherein the first, second, third, fourth, ninth and twelfth transistors are pnp transistors, and the fifth, sixth, seventh, eighth, tenth and eleventh transistors are npn transistors.

10 ✓ 20. A method of amplifying a signal, comprising the steps of:
 biasing a plurality of transistors in a pre-driver sub-stage;
 biasing a plurality of transistors in a final sub-stage;
 routing the positive cycle of the signal through a first, biased pre-driver sub-stage circuit;
15 routing the negative cycle of the signal through a second, biased pre-driver sub-stage circuit;
 amplifying the positive cycle of the signal in the first, biased pre-driver sub-stage circuit;
 amplifying the negative cycle of the signal in the second, biased pre-driver sub-stage circuit;
20 routing the amplified positive cycle of the signal to a first, biased final sub-stage circuit;
 routing the amplified negative cycle of the signal to a second, biased final sub-stage circuit;

5 further amplifying the positive cycle of the signal in a first, biased
final sub-stage circuit in tandem with the pre-driver sub-stage amplification action;
further amplifying the negative cycle of the signal in a second, final
sub-stage circuit in tandem with the pre-driver sub-stage amplification action;
employing a plurality of translinear loops in the pre-driver sub-stage
10 circuits and final sub-stage circuits so as to preserve the amplitude, frequency and
phase characteristics of the signals during routing and amplification; and
joining in phase the amplified portions of the positive and negative
signal at an output stage terminal in a manner that results in high linearity and low
distortion of an output signal when compared to the input signal

15 21. The method of amplifying a signal recited in Claim 20, further
comprising the step of feeding back a portion of the signal in a localized feedback
system to extend bandwidth.

✓ 22. A method of amplifying signals in an operational amplifier
output stage, comprising the steps of:

20 generating bias currents in a pre-driver sub-stage and a final sub-stage;
inputting the signals into the pre-driver sub-stage and a final sub-stage;
amplifying the signals in tandem in the pre-driver sub-stage and final sub-
stage;

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loops in the pre-drive
loss in the pre-drive
so as to achieve hi
d to the input sign

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